HIGH DATA RATE SPREAD SPECTRUM TRANSCEIVER AND ASSOCIATED METHODS

FIELD OF THE INVENTION

The invention relates to the field of communication electronics, and, more particularly, to a spread spectrum transceiver and associated methods.

BACKGROUND OF THE INVENTION

Wireless or radio communication between separated electronic devices is widely used. For example, a wireless local area network (WLAN) is a flexible data communication system that may be an extension to, or an alternative for, a wired LAN within a building or campus. A WLAN uses radio technology to transmit and receive data over the air, thereby reducing or minimizing the need for wired connections. Accordingly, a WLAN combines data connectivity with user mobility, and, through simplified configurations, also permits a movable LAN.

Over the past several years, WLANs have gained acceptance among a number users including, for example, healthcare, retail, manufacturing, warehousing, and academic areas. These groups have benefited from the productivity gains of using hand-held terminals and notebook computers, for example, to transmit real-time information to centralized hosts for processing. Today WLANs are becoming more widely recognized and used as a general purpose connectivity alternative for an even broader range of users. In addition, a WLAN provides installation flexibility and permits a computer network to be used in situations where wireline technology is not practical.

In a typical WLAN, an access point provided by a transceiver, that is, a combination transmitter and receiver, connects to the wired network from a fixed location. Accordingly, the access transceiver receives, buffers, and transmits data between the WLAN and the wired network. A single access transceiver can support a small group of collocated users within a range of less than about one hundred to several hundred feet. The end users connect to the WLAN through transceivers which are typically implemented as PC cards in a notebook computer, or ISA or PCI cards for desktop computers. Of course the transceiver may be integrated with any device, such as a hand-held computer.

The assignee of the present invention has developed and manufactured a set of integrated circuits for a WLAN under the mark PRISM 1 which is compatible with the proposed IEEE 802.11 standard. The PRISM 1 chip set is further described in Harris Corporation Application Note entitled "Harris PRISM Chip Set", No. AN9614, March 1996; and also in a publication entitled "PRISM 2.4 GHz Chip Set", file no. 4063.4, October 1996.

The PRISM 1 chip set provides all the functions necessary for full or half duplex, direct sequence spread spectrum, packet communications at the 2.4 to 2.5 GHz ISM radio band. In particular, the HSP3824 baseband processor manufactured by Harris Corporation employs quadrature or bi-phase phase shift keying (QPSK or BPSK) modulation schemes. While the PRISM 1 chip set is operable at 2 Mbit/s for BPSK and 4 Mbit/s for QPSK, these data rates may not be sufficient for higher data rate applications.

Spread spectrum communications have been used for various applications, such as cellular telephone communications, to provide robustness to jamming, good interference and multi-path rejection, and inherently secure

communications from eavesdroppers, as described, for example, in U.S. Pat. No. 5,515,396 to Dalekotzin. The patent discloses a code division multiple access (CDMA) cellular communication system using four Walsh spreading codes to allow transmission of a higher information rate without a substantial duplication of transmitter hardware. U.S. Pat. No. 5,535,239 to Padovani et al., U.S. Pat. No. 5,416,797 to Gilhousen et al., U.S. Pat. No. 5,309,474 to Gilhousen et al., and U.S. Pat. No. 5,103,459 to Gilhousen et al. also disclose a CDMA spread spectrum cellular telephone communications system using Walsh function spreading codes.

Unfortunately, the conventional Walsh function spreading codes may create undesirable signal components for some applications. Moreover, a WLAN application, for example, may require a change between BPSK and QPSK during operation, that is, on-the-fly. Spreading codes may be difficult to use in such an application where an on-the-fly change is required.

SUMMARY OF THE INVENTION

In view of the foregoing background, it is therefore an object of the present invention to provide a spread spectrum transceiver and associated method permitting operation at higher data rates than conventional transceivers.

It is another object of the invention to provide a spread spectrum transceiver and associated method to permit operation at higher data rates and which may switch on-the-fly between different data rates and/or formats.

These and other objects, features and advantages in accordance with the invention are provided by a spread spectrum radio transceiver comprising a high data rate baseband processor and a radio circuit connected thereto. The baseband processor preferably includes a modulator for spread spectrum phase shift keying (PSK) modulating information for transmission via the radio circuit, and wherein the modulator, in one embodiment, comprises at least one modified Walsh code function encoder for encoding information according to a modified Walsh code. The baseband processor also preferably further comprises a demodulator for spread spectrum PSK demodulating information received from the radio circuit. The demodulator is preferably connected to the output of at least one analog-to-digital (A/D) converter, which, in turn, is AC-coupled to the associated receive portions of the radio circuit. Accordingly, the demodulator preferably comprises at least one modified Walsh code function correlator for decoding information according to the modified Walsh code. The modified Walsh code substantially reduces an average DC component which in combination with the AC-coupling to the at least one A/D converter thereby increases overall system performance. Other orthogonal and bi-orthogonal coding schemes may also be used, wherein the average DC component is preferably substantially reduced or avoided.

The modulator preferably comprises means for operating in one of a bi-phase PSK (BPSK) modulation mode at a first data rate defining a first format, and a quadrature PSK (QPSK) mode at a second data rate defining a second format. In addition, the demodulator preferably comprises means for operating in one of the first and second formats. The modulator may also preferably include header modulator means for modulating data packets to include a header at a predetermined modulation and a third data rate defining a third format, and for modulating variable data at one of the first and second formats. Accordingly, the demodulator thus preferably includes header demodulator means for demodu-

lating data packets by demodulating the header at the third format and for switching to either the first and second formats of the variable data after the header. The third format is preferably differential BPSK, and the third data rate is preferably lower than the first and second data rates.

The demodulator may preferably comprise first and second carrier tracking loops—the first carrier tracking loop for the third format, and the second carrier tracking loop for the first and second formats. The second carrier tracking loop, in turn, may comprise a carrier numerically controlled oscillator (NCO), and NCO control means for selectively operating the carrier NCO based upon a carrier phase of the first carrier tracking loop to thereby facilitate switching to the format of the variable data. The second carrier tracking loop may also comprise a carrier loop filter, and carrier loop filter control means for selectively operating the carrier loop filter based upon a frequency of the first carrier tracking loop to facilitate switching to the format of the variable data. The carrier tracking loops permit switching to the desired format after the header and on-the-fly.

The at least one modified Walsh code function correlator of the demodulator preferably comprises a modified Walsh function generator, and a plurality of parallel connected correlators connected to the modified Walsh function generator. The modified Walsh code may be a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto. In addition, the modulator in one embodiment preferably further comprises means for partitioning data into four bit nibbles of sign (one bit) and magnitude (three bits) to the modified Walsh code function encoder.

The modulator may also include spreading means for spreading each data bit using a pseudorandom (PN) sequence at a predetermined chip rate. Accordingly, the modulator may also comprise preamble modulating means for generating a preamble, and wherein the demodulator includes preamble demodulator means for demodulating the preamble for achieving initial PN sequence synchronization.

The modulator for the spread spectrum transceiver may include a scrambler, and the demodulator accordingly preferably includes a descrambler. The demodulator may also include clear channel assessing means for generating a clear channel assessment signal to facilitate communications only when the channel is clear.

The baseband processor is desirably coupled to a radio circuit for the complete spread spectrum transceiver. Accordingly, the transceiver preferably includes a quadrature intermediate frequency modulator/demodulator connected to the baseband processor, and an up/down frequency converter connected to the quadrature intermediate frequency modulator/demodulator. In addition, the radio circuit preferably further comprises a low noise amplifier having an output connected to an input of the up/down converter, and a radio frequency power amplifier having an input connected to an output of the up/down converter. The spread spectrum radio transceiver preferably also includes an antenna, and an antenna switch for switching the antenna between the output of the radio frequency power amplifier and the input of the low noise amplifier.

A method aspect of the invention is for baseband processing for spread spectrum radio communication. The method preferably comprises the steps of: spread spectrum phase shift keying (PSK) modulating information for transmission by encoding information according to a predetermined bi-orthogonal code for reducing an average DC signal component; and spread spectrum PSK demodulating received information by decoding information according to the predetermined bi-orthogonal code. The predetermined bi-orthogonal code is preferably a modified Walsh function code.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic circuit diagram of a transceiver in accordance with the present invention.

FIG. **2** is a schematic circuit diagram of a modulator portion of the high data rate baseband processor in accordance with the present invention.

FIG. **3** is a timing diagram of signals generated by the present invention.

FIG. **4** is a timing diagram of additional signals generated by the present invention.

FIG. **5** is a schematic circuit diagram of a demodulator portion of the high data rate baseband processor in accordance with the present invention.

FIG. **6** is a schematic circuit diagram of the correlator portion of the demodulator of the high data rate baseband processor in accordance with the present invention.

FIG. **7** is a schematic circuit diagram of additional portions of the demodulator of the high data rate baseband processor in accordance with the present invention.

FIG. **8** is a schematic circuit diagram of further portions of the demodulator of the high data rate baseband processor in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout.

Referring to FIG. **1**, a wireless transceiver **30** in accordance with the invention is first described. The transceiver **30** may be readily used for WLAN applications in the 2.4 GHz ISM band in accordance with the proposed IEEE 802.11 standard. Those of skill in the art will readily recognize other applications for the transceiver **30** as well. The transceiver **30** includes the selectable antennas **31** coupled to the radio power amplifier and TX/RX switch **32** as may be provided by a Harris part number HFA3925. As would be readily understood by those skilled in the art, multiple antennas may be provided for space diversity reception.

A low noise amplifier **38**, as may be provided by Harris part number HFA3424, is also operatively connected to the antennas. The illustrated up/down converter **33** is connected to both the low noise amplifier **38** and the RF power amplifier and TX/RX switch **32** as would be readily understood by those skilled in the art. The up/down converter **33** may be provided by a Harris part number HFA3624, for example. The up/down converter **33**, in turn, is connected to the illustrated dual frequency synthesizer **34** and the quad IF modulator/demodulator **35**. The dual synthesizer **34** may be a Harris part number HFA3524 and the quad IF modulator **35** may be a Harris part number HFA3724. All the components described so far are included in a 2.4 GHz direct sequence spread spectrum wireless transceiver chip set

manufactured by Harris Corporation under the designation PRISM 1. Various filters **36**, and the illustrated voltage controlled oscillators **37** may also be provided as would be readily understood by those skilled in the art and as further described in the Harris PRISM 1 chip set literature, such as the application note No. AN9614, March 1996, the entire disclosure of which is incorporated herein by reference.

Turning now more particularly to the right hand side of FIG. **1**, the high data rate direct sequence spread spectrum (DSS) baseband processor **40** in accordance with the present invention is now described. The conventional Harris PRISM 1 chip set includes a low data rate DSS baseband processor available under the designation HSP3824. This prior baseband processor is described in detail in a publication entitled "Direct Sequence Spread Spectrum Baseband Processor, March 1996, file number 4064.4, and the entire disclosure of which is incorporated herein by reference.

Like the HSP3824 baseband processor, the high data rate baseband processor **40** of the invention contains all of the functions necessary for a full or half duplex packet baseband transceiver. The processor **40** has on-board dual 3-bit A/D converters **41** for receiving the receive I and Q signals from the quad IF modulator **35**. Also like the HSP3824, the high data rate processor **40** includes a receive signal strength indicator (RSSI) monitoring function with the on-board 6-bit A/D converter and CCA circuit block **44** provides a clear channel assessment (CCA) to avoid data collisions and optimize network throughput as would be readily understood by those skilled in the art.

The present invention provides an extension of the PRISM 1 product from 1 Mbit/s BPSK and 2 Mbit/s QPSK to 5.5 Mbit/s BPSK and 11 Mbit/s QPSK. This is accomplished by keeping the chip rate constant at 11 Mchip/s. This allows the same RF circuits to be used for higher data rates. The symbol rate of the high rate mode is 11 MHz/8=1.375 Msymbol/s.

For the 5.5 Mbit/s mode of the present invention, the bits are scrambled and then encoded from 4 bit nibbles to 8 chip modified Walsh functions. This mapping results in bi-orthogonal codes which have a better bit error rate (BER) performance than BPSK alone. The resulting 11 Mchip/s data stream is BPSK modulated. The demodulator comprises a modified Walsh correlator and associated chip tracking, carrier tracking, and reformatting devices as described in greater detail below.

For the 11 Mbit/s mode, the bits are scrambled and then encoded from 4 bit nibbles to 8 chip modified Walsh functions independently on each I and Q rail. There are 8 information bits per symbol mapped to 2 modified Walsh functions. This mapping results in bi-orthogonal codes which have better BER performance than QPSK alone. The resulting two 11 Mchip/s data streams are QPSK modulated.

The theoretical BER performance of this type of modulation is approximately 10^{-5} at an Eb/No of 8 dB versus 9.6 dB for plain BPSK or QPSK. This coding gain is due to the bi-orthogonal coding. There is bandwidth expansion for all of the modulations to help combat multi-path and reduce the effects of interference.

Referring additionally to FIG. **2**, the output of the QPSK/BPSK modulator and scrambler circuit **51** is partitioned into nibbles of Sign-Magnitude of 4 bits, with the least significant bit (LSB) first. For QPSK, 2 nibbles are presented in parallel to the Modified Walsh Generators **53***a*, **53***b*—the first nibble from the B serial-in/parallel-out SIPO circuit block **52***b* and the second from A SIPO **52***a*. The two nibbles form a symbol of data. The bit rate may be 11 Mbit/s as illustrated. Therefore, the symbol rate is 1.375 Mbit/s (11/8=1.375). For BPSK, nibbles are presented from the A SIPO **52***a* only. The B SIPO **52***b* is disabled. A nibble forms a symbol of data. The bit rate in this instance is 5.5 Mbit/s and the symbol rate remains 1.375 Mbit/s (5.5/4=1.375).

The Magnitude part of the SIPO output points to one of the Modified Walsh Sequences shown in the table below, along with the basic Walsh sequences for comparison.

MAG	BASIC WALSH	MODIFIED WALSH
0	00	03
1	0F	0C
2	33	30
3	3C	3F
4	55	56
5	5A	59
6	66	65
7	69	6A

The Sel Walsh A_n and Sel Walsh B bits from the clock enable logic circuit **54** multiplex the selected Walsh sequence to the output, and wherein the LSBs are output first. The A Sign and B Sign bits bypass the respective Modified Walsh Generators **53***a*, **53***b* and are XOR'd to the sequence.

As would be readily understood by those skilled in the art, there are other possible mappings of bits to Walsh symbols that are contemplated by the present invention. In addition, the Modified Walsh code may be generated by modulo two adding a fixed hexadecimal code to the basic or standard Walsh codes to thereby reduce the average DC signal component and thereby enhance overall performance as will be explained in greater detail below.

The output of the Diff encoders of the last symbol of the header CRC is the reference for the high rate data. The header may always be BPSK. This reference is XOR'd to I and Q signals before the output. This allows the demodulator **60**, as described in greater detail below, to compensate for phase ambiguity without Diff decoding the high rate data. Data flip flops **55***a*, **55***b* are connected to the multiplexer, although in other embodiments the flip flops may be positioned further downstream as would be readily understood by those skilled in the art. The output chip rate is 11 Mchip/s. For BPSK, the same chip sequence is output on each I and Q rail via the multiplexer **57**. The output multiplexer **58** provides the selection of the appropriate data rate and format.

Referring now additionally to FIG. **3**, the timing and signal format for the interface **80** is described in greater detail. Referring to the left hand portion, Sync is all 1's, and SFD is F3AOh for the PLCP preamble **90**. Now relating to the PLCP header **91**, the SIGNAL is:

0Ah	1 Mbit/s BPSK,
14h	2 Mbit/S QPSK,
37h	5.5 Mbit/s BPSK, and
6Eh	11 Mbit/s QPSK.

The SERVICE is OOh, the LENGTH is XXXXh wherein the length is in μs, and the CRC is XXXXh calculated based on SIGNAL, SERVICE and LENGTH. MPDU is variable with a number of octets (bytes).

The PLCP preamble and PLCP header are always at 1 Mbit/s, Diff encoded, scrambled and spread with an 11 chip barker. SYNC and SFD are internally generated. SIGNAL, SERVICE and LENGTH fields are provided by the interface